Si Nanoelectronic Device Technology

November 30, 2009

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My research standing point and aim

Contribute to our human society through developing new electronic device technology.

Still our society does need the improvement of electronic device for power consumption and performance, as well as new function.

My research standing point and aim

Develop the technologies for which not many people are participating now, and which are very difficult and challenging, but which I believe to be the key and mainstream after 10 – 25 years.

For integrated circuit technology, there are still strong demands for decreasing power consumption, and increasing performance as you can see for center and also for your own PC.

What we can do from integrated circuit side?

Solution is not in so-called ‘beyond CMOS’ technology, but in the extension mainstream CMOS technology.

Extension of mainstream technology will take care the problems for another 20 years.

What I can contribute in the extension mainstream CMOS technology which will be realized in 25 years.

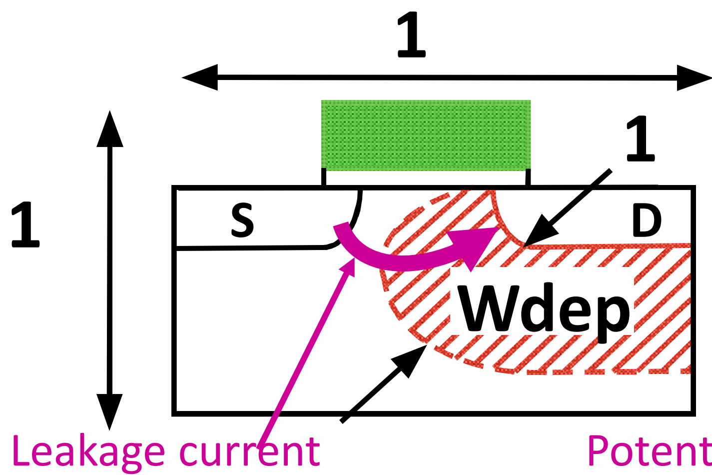
We selected challenging items.

1. High-k with EOT less than 0.5 nm

2. Si nanowire FET

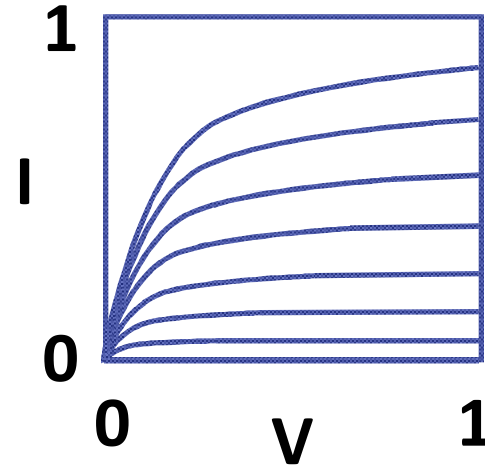
3. Si nanowire FET

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



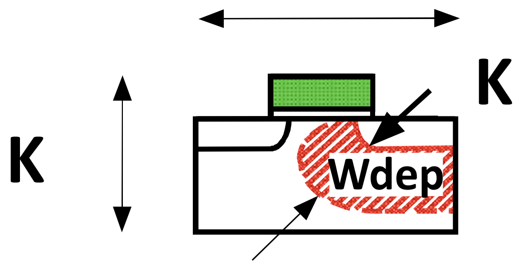
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

X , Y , Z : K, V : K, Na : 1/K

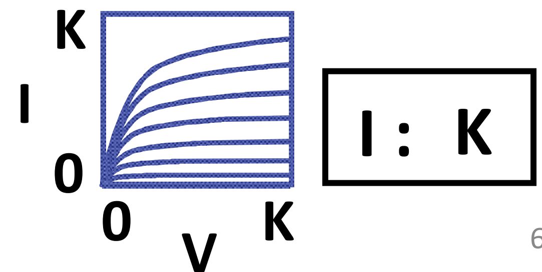
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$

: K



I : K

Scaling down approach is very beautiful and imprtant

2 Generations scaling	$k = 0.7^2 = 0.5$ if we keep the chip area the same for scaling
Single MOFET	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → $1/0.5 = 2$ P (Power) → 1

- The concerns for limits of down-scaling have been announced for every generation.

- However, down-scaling of CMOS is still the ‘royal road’* for high performance and low power.

- Effort for the down-scaling has to be continued by all means.

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*Euclid of Alexandria (325BC?-265BC?)

‘There is no royal road to Geometry’

Mencius (Meng-zi), China (372BC?-289BC?)

孟子: 王道, 覇道 (Rule of right vs. Rule of military)

-There will be still 4~6 generations left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

Baseline CMOS | Ultimately Scaled CMOS | Functionally Enhanced CMOS | Nanowire Electronics | Ferromagnetic Logic Devices | Spin Logic Devices

32nm | 22nm | 16nm | 11nm | 8nm | 5.5nm?*

Multiple gate MOSFETs
Channel Replacement Materials
Low Dimensional Materials Channels

3 important innovations

New State Variable
New Devices
New Data Representation
New Data Processing Algorithms

"More Moore" "Beyond CMOS"

ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

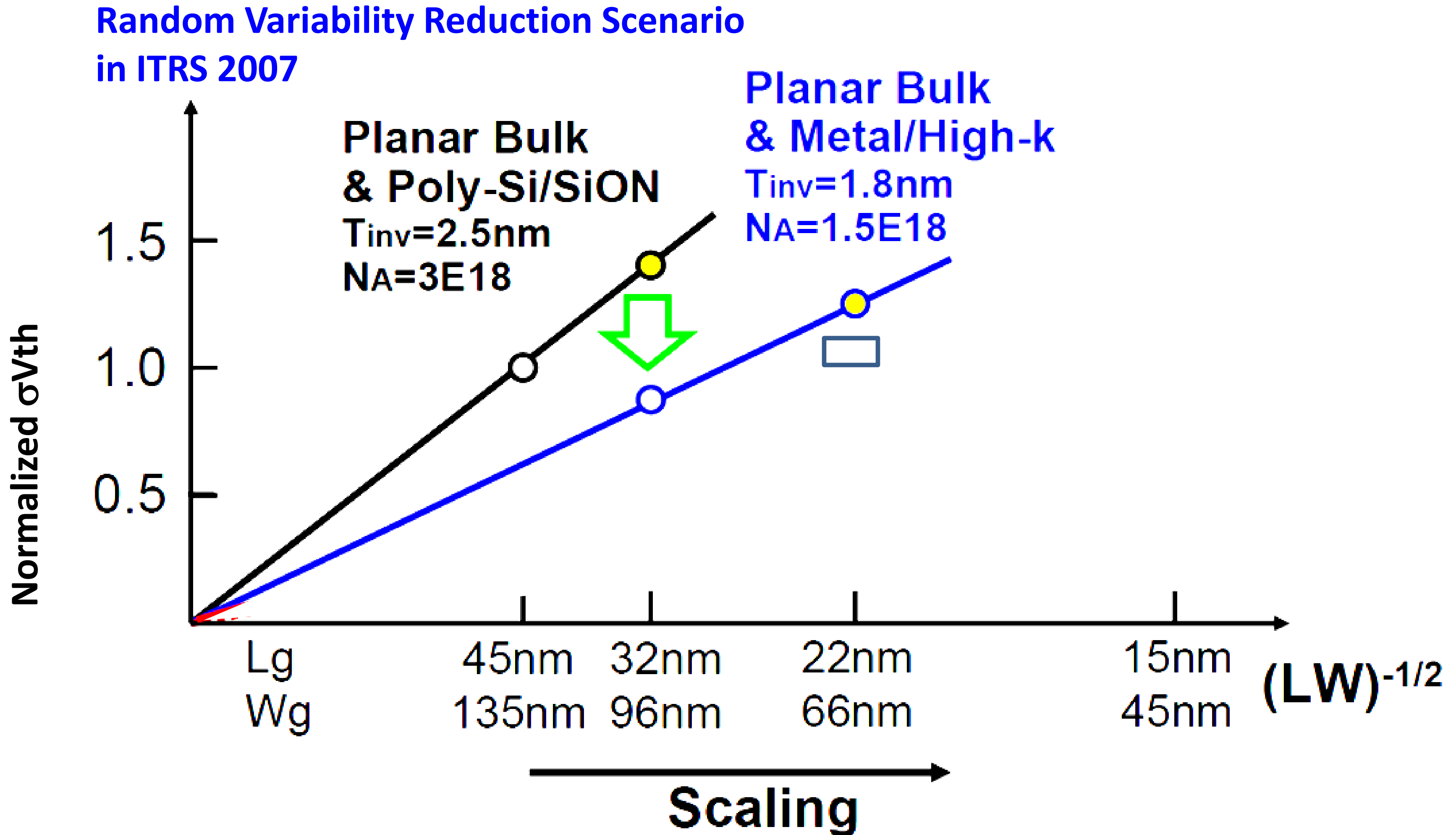
*5.5nm? was added by Iwai

Before reaching the scaling limit, we need to pursuit the down scaling limit, introducing new materials such as (1) high-k.

Then, (2) Si-nanowire and (3) Alternative channel (III-V and Ge) .

That is why I am concentrating the research of The above 3 – (1), (2), (3).

Gate oxide scaling is very important also for suppressing the variation.

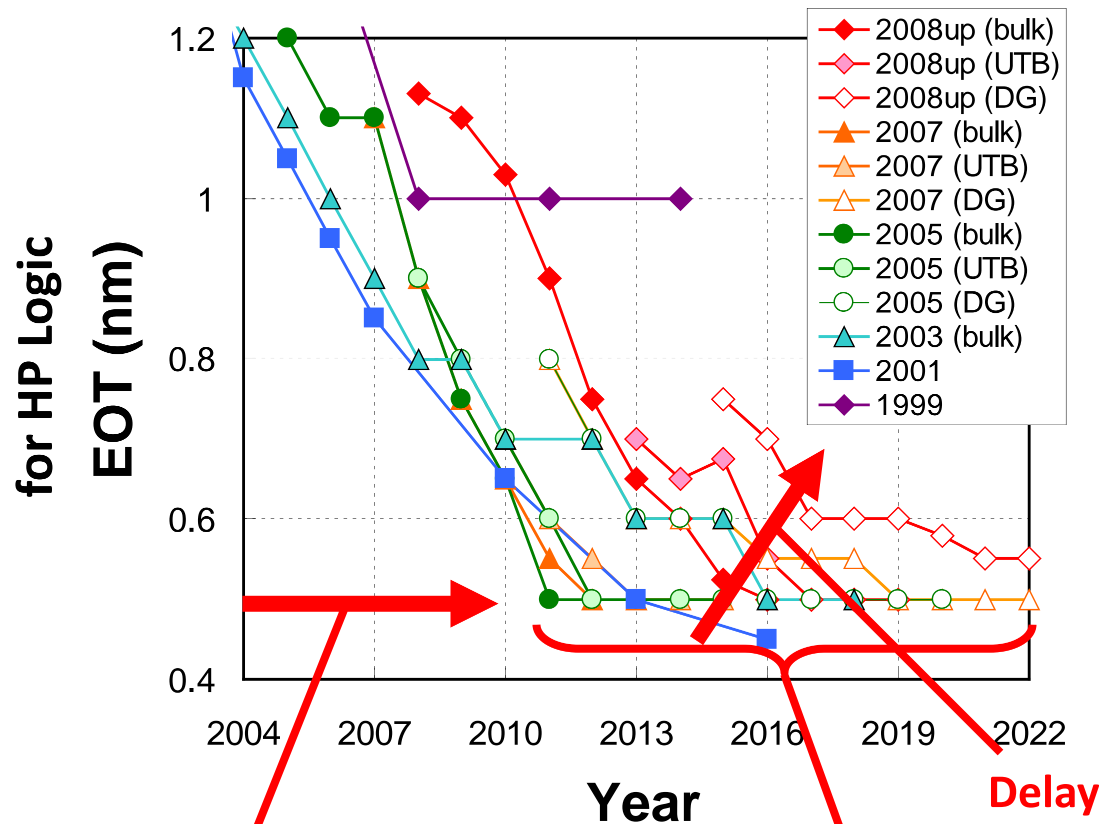


Assumption: Random dopant fluctuation is Main source of Random Variability: Line width roughness of Lg and Wg is not considered in this

Source: 2007 ITRS Winter Public Conf.

EOT (Equivalent gate oxide thickness) is supposed to saturate at 0.5

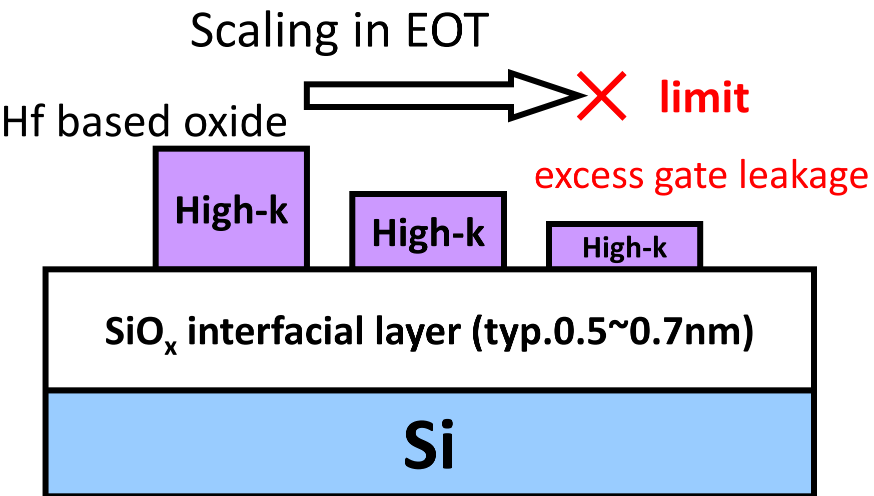
Saturation of EOT thinning is a serious roadblock to proper down-scaling → short-channel effect & Vth variation

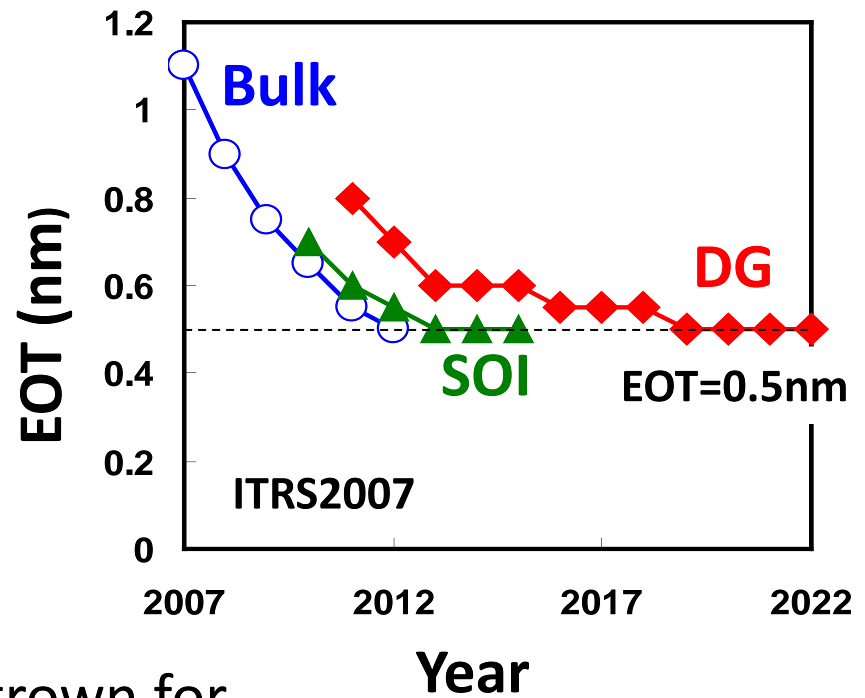


Is 0.5nm real limit?

Saturation

High-k for Further Scaling

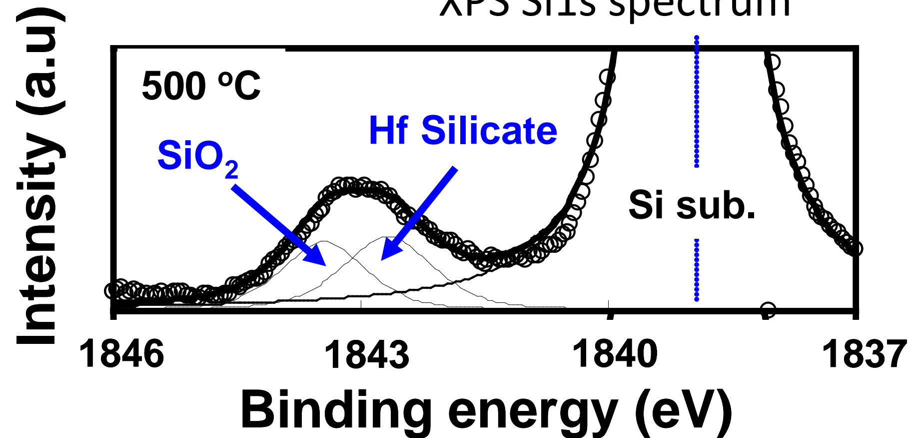




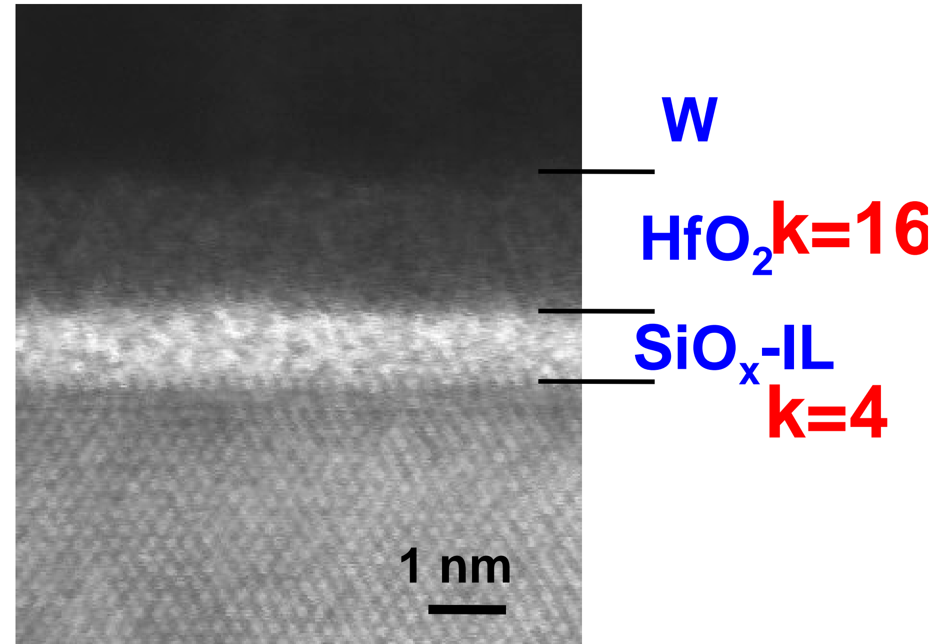
SiO_2 interfacial layer inserted or re-grown for
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

- **SiO_2-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm**
- **EOT scaling is expected down to 0.5 nm in ITRS**

SiO_x-IL growth at HfO_2/Si Interface

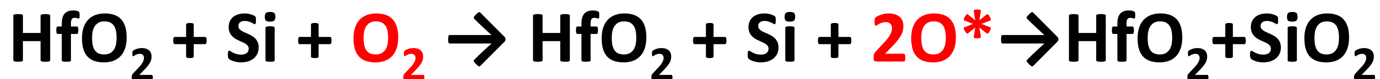


TEM image 500 °C 30min

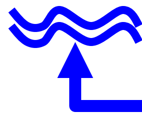


Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$



H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

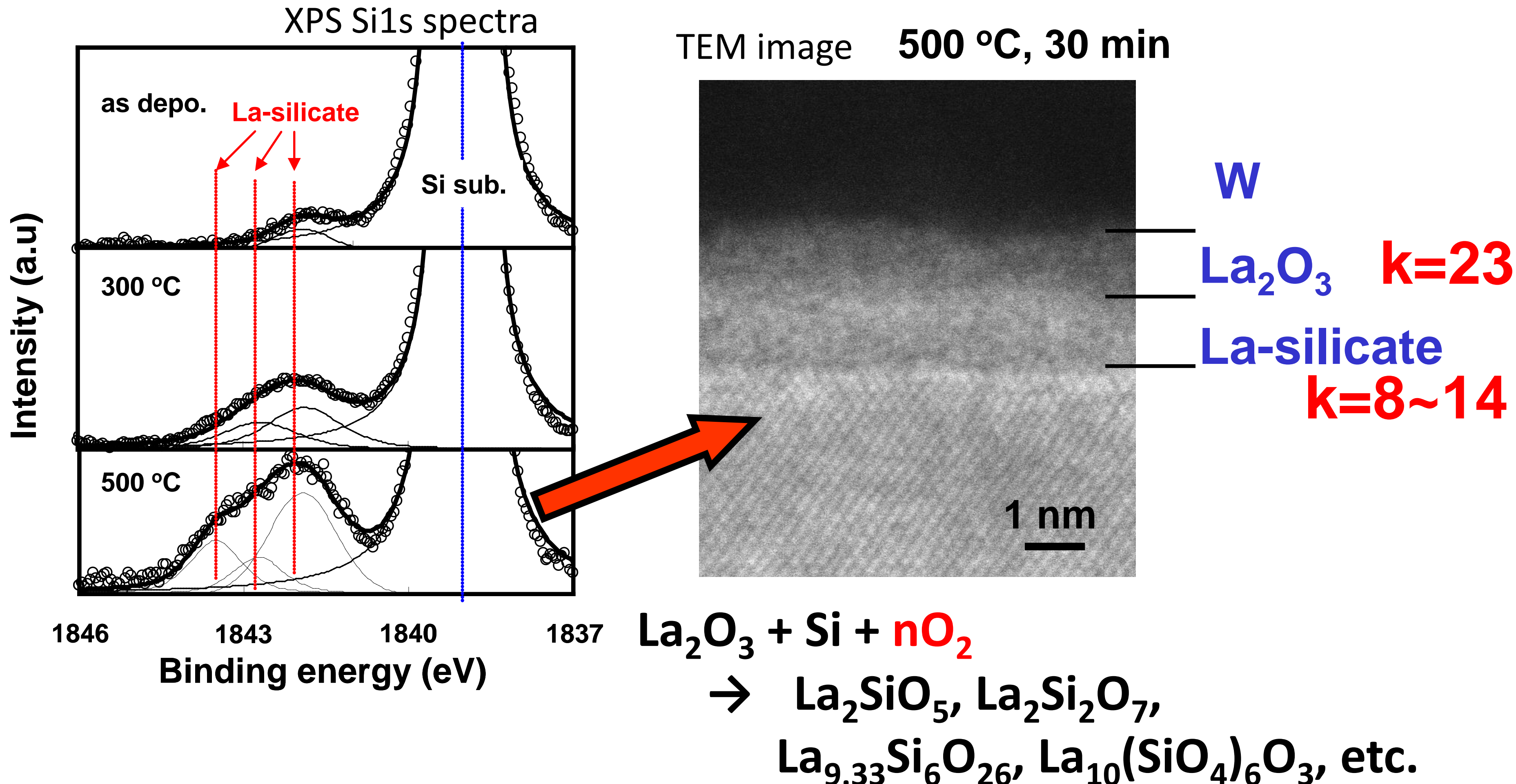
D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible



La_2O_3 can achieve direct contact of high-k/Si

EOT<0.5nm with Gain in Drive Current

(a) EOT=0.37nm V_{th}=-0.04V

W/L=50/2.5μm
PMA 300ºC (30min)

insufficient compensation region

Drain current (mA)

3.5 3 2 1 0

0 0.2 0.4 0.6 0.8 1

Drain voltage (V)

(b) EOT=0.43nm V_{th}=-0.03V

4%up

0 0.2 0.4 0.6 0.8 1

Drain voltage (V)

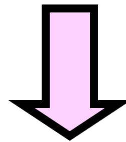
(c) EOT=0.48nm V_{th}=-0.02V

14%up

0 0.2 0.4 0.6 0.8 1

Drain voltage (V)

14% of I_d increase is observed even at saturation region

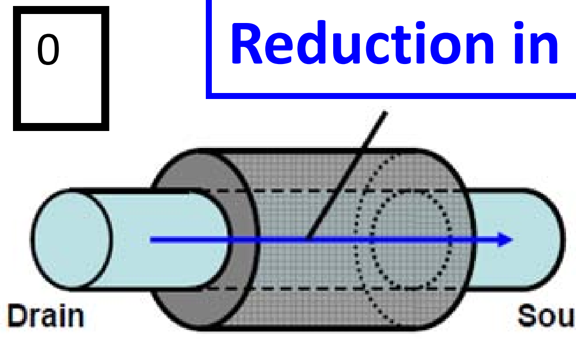


EOT below 0.4nm is still useful for scaling

Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

Source: Y. Lee., T. Nagata., K. Kakushima., K. Shiraishi, and H. Iwai, IWDTF 2008, Tokyo, November, 2008



0 **Reduction in Ioff (Isd-leak)**

Good control of Isd-leak by surrounding gate

Trade off

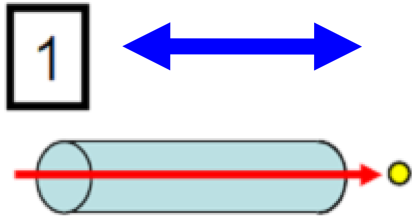
Carrier scattering probability

Small **Large**

# of quantum channel

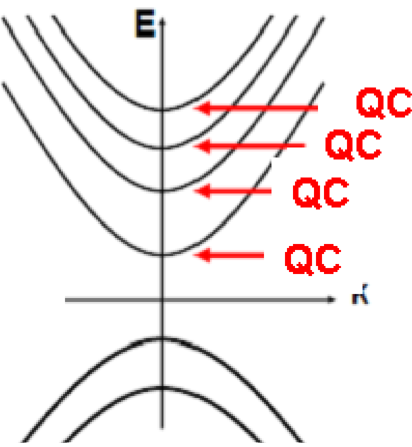
Small **Large**

Increase in Ion (Id-sat)



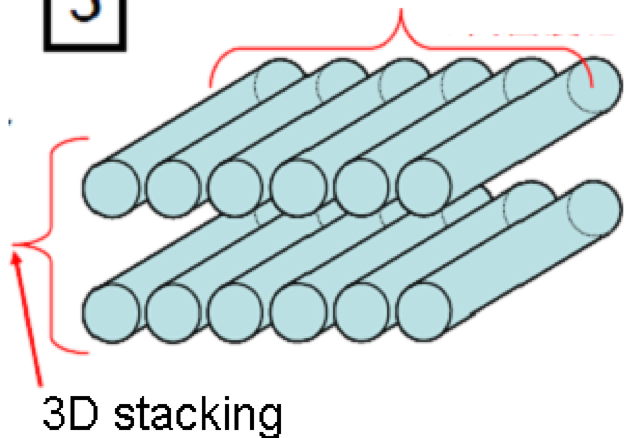
High Conduction (1D)

Go=77.8μS/wire



Multiple quantum channel (QC) used for conduction

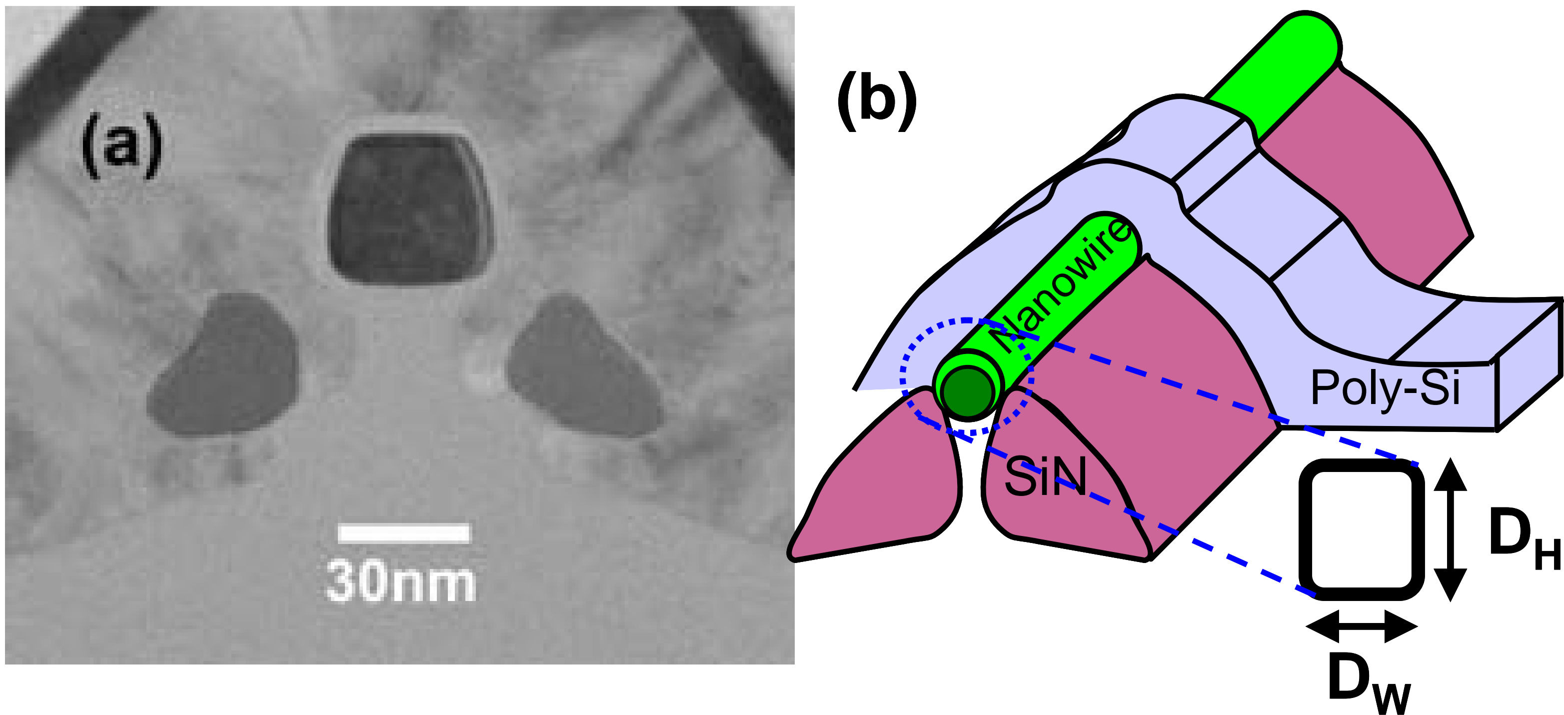
3



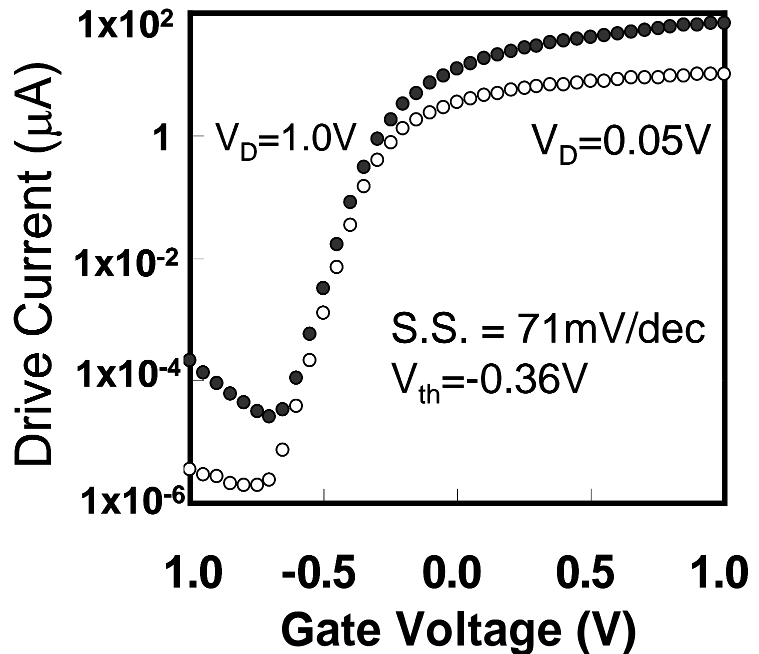
High-density lateral and vertical integration

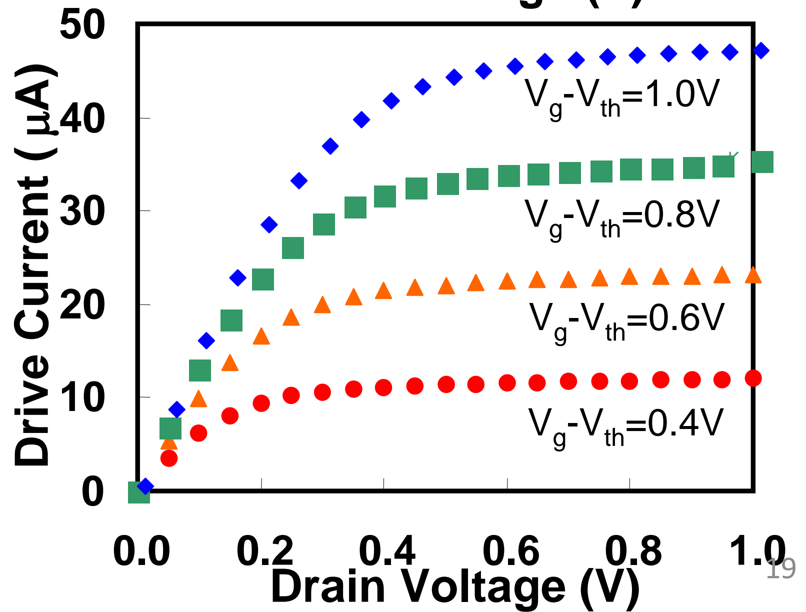
Source: T. Ohno, K. Shiraishi, and T. Ogawa, Phys. Rev. Lett. ,1992

(a) A cross sectional TEM image of Si NW FET in this work. Oxide support still remains thanks to nanowire sidewall (SiN). Semi-Around gate structure, nearby 300 degree of whose channel is surrounded by gate oxide and poly-Si electrode. Schematic illustration is shown in upper-right.



D_W=25nm and D_H=35nm.
Fairly nice I_{on}/I_{off} ratio of 10^7 with a low subthrshold slope of 71mV/dec. has been obtained.





Effective electron mobility of [110]-directed multi channel Si NW FET in this work. (D_W=25nm, D_H=35nm)